LOW SKEW, 1-4 DIFFERENTIAL-TO-LVDS FANOUT BUFFER

ICS854104

General Description

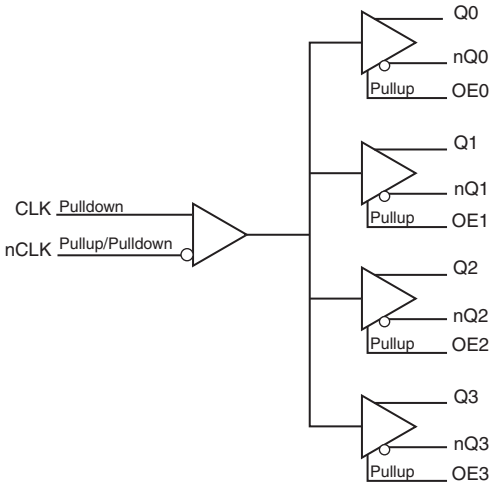
The ICS854104 is a low skew, high performance 1-to-4 Differential-to-LVDS Clock Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. Utilizing Low Voltage Differential Signaling (LVDS), the ICS854104 provides a low power, low noise, solution for distributing clock signals over controlled impedances of 100Ω. The ICS854104 accepts a differential input level and translates it to LVDS output levels.

Guaranteed output and part-to-part skew characteristics make the ICS854104 ideal for those applications demanding well defined performance and repeatability.

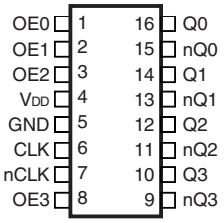
Features

- Four LVDS outputs
- One differential clock input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Each output has an individual OE control
- Maximum output frequency: 700MHz
- Translates differential input signals to LVDS levels
- Additive phase jitter, RMS: 0.1ps (typical)
- Output skew: TBD
- Part-to-part skew: TBD
- Propagation delay: 1.1ns (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS854104
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	OE0	Input	Pullup	Output enable pin for Q0, nQ0 output. If OE pin is LOW, outputs will drive HiZ. LVCMOS/LVTTL interface levels.
2	OE1	Input	Pullup	Output enable pin for Q1, nQ1 outputs. If OE pin is LOW, outputs will drive HiZ. LVCMOS/LVTTL interface levels.
3	OE2	Input	Pullup	Output enable pin for Q2, nQ2 outputs. If OE pin is LOW, outputs will drive HiZ. LVCMOS/LVTTL interface levels.
4	V_{DD}	Power		Positive supply pin.
5	GND	Power		Power supply ground.
6	CLK	Input	Pulldown	Non-inverting differential clock input.
7	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
8	OE3	Input	Pullup	Output enable pin for Q3, nQ3 outputs. If OE pin is LOW, outputs will drive HiZ. LVCMOS/LVTTL interface levels.
9, 10	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
11, 12	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
13, 14	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
15, 16	nQ0, Q0	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3. OE[3:0] FUNCTION TABLE

Inputs	Outputs
OE[3:0]	**Q0/nQ0:Q3/nQ3**
0	HiZ (default)
1	Active

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			60		mA

Table 4B. LVCMOS / LVTTL DC Characteristics, V_{DD} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

NOTE: Outputs terminated with 50Ω to $V_{DD}/2$. See Parameter Measurement Information, "Output Load Test Circuit".

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4C. LVDS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

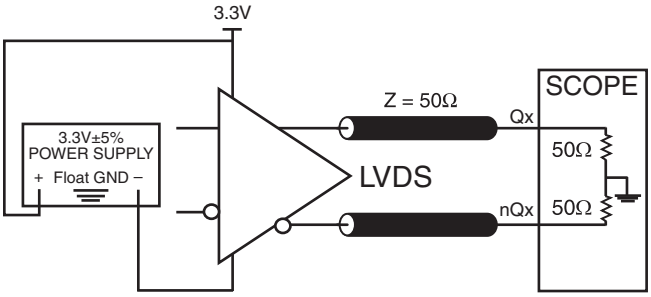
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			30		mV
V_{OS}	Offset Voltage			1.3		V
ΔV_{OS}	V_{OS} Magnitude Change			20		mV

TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

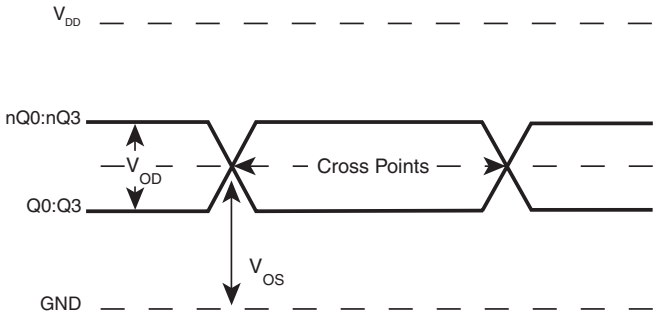
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1			1.1		ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	(12kHz to 20MHz)		0.1		ps
*t*sk(o)	Output Skew; NOTE 2, 4			TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		400		ps
odc	Output Duty Cycle			50		%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the V_{DD}/2 of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DD}/2 of the input to the differential output crossing point.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

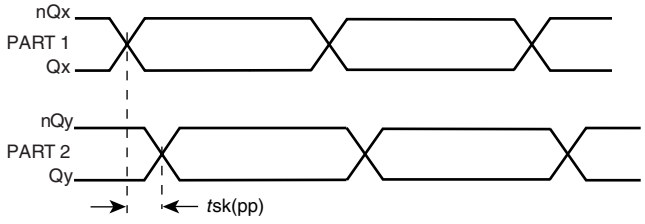
PARAMETER MEASUREMENT INFORMATION



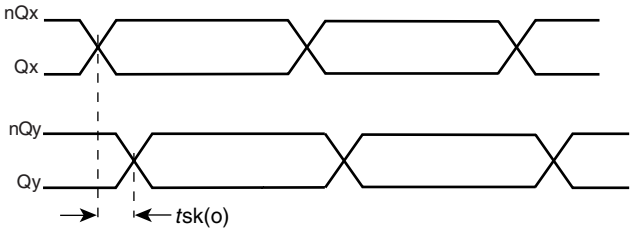
3.3V OUTPUT LOAD AC TEST CIRCUIT



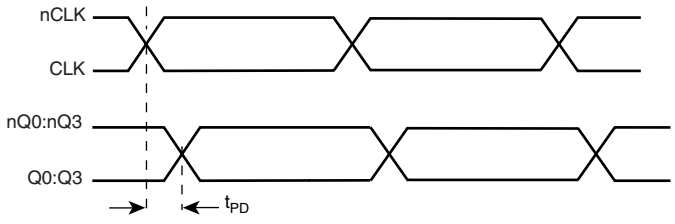
DIFFERENTIAL OUTPUT LEVEL



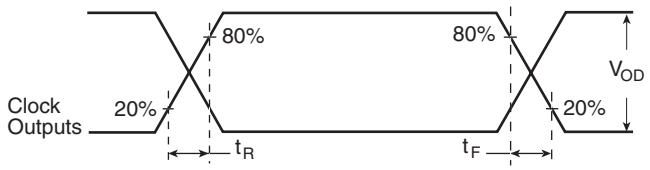
PART-TO-PART SKEW



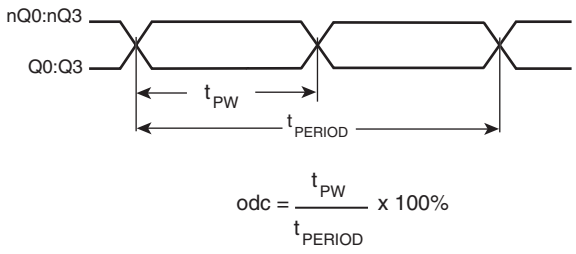
OUTPUT SKEW



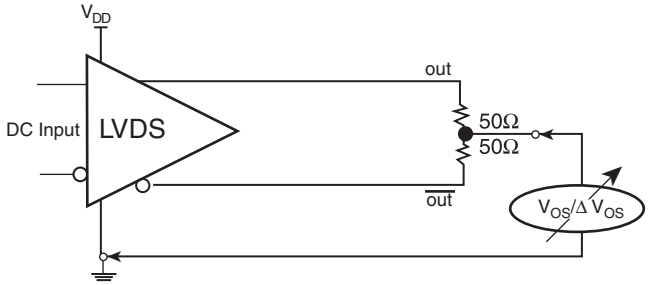
PROPAGATION DELAY



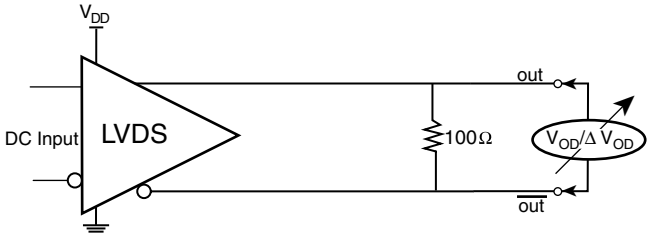
OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OFFSET VOLTAGE



DIFFERENTIAL OUTPUT VOLTAGE

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD}= 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

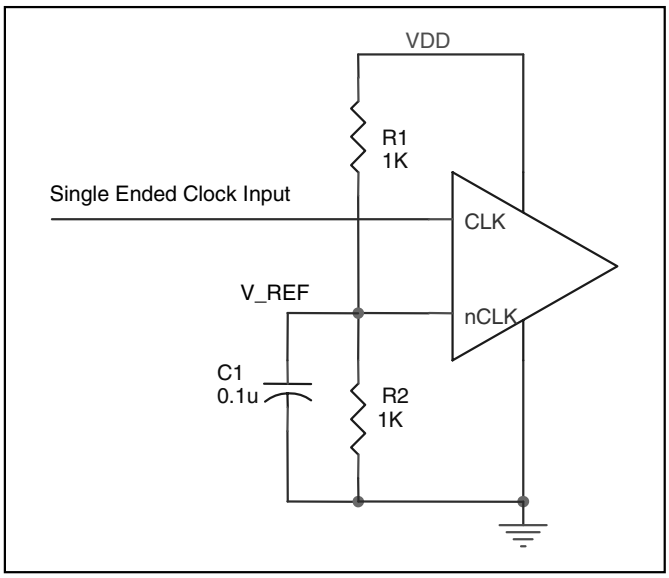


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVDS

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 2.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

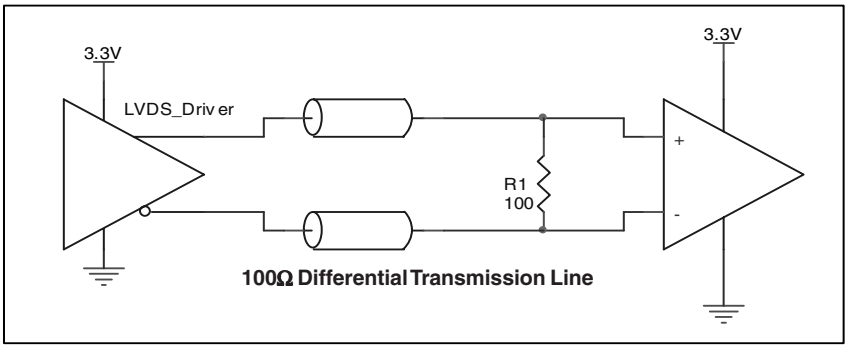


Figure 2. Typical LVDS Driver Termination

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS854104 is: 286

Pin compatible with SN65LVDS104

Package Outline - G Suffix for 16 Lead TSSOP

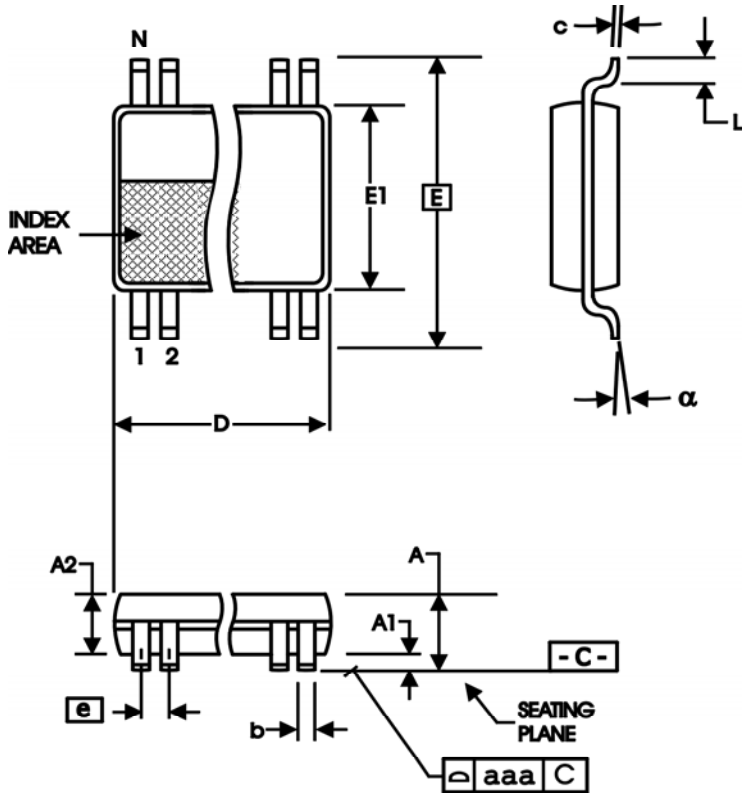


Table 7. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS854104AG	854104AG	16 Lead TSSOP	tube	0°C to 70°C
ICS854104AGT	854104AG	16 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS854104AGLF	TBD	16 Lead TSSOP	tube	0°C to 70°C
ICS854104AGLFT	TBD	16 Lead TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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